(12) UK Patent Application (19) GB (11) 2 076 547 A

(21) Application No 8112542
(22) Date of filing 23 Apr 1981
(30) Prlority data
(31) 150412
(32) 16 May 1980
(33) United States of America (US)
(43) Application published 2 Dec 1981
(51) INT CL³ G01R 27/14
(52) Domestic classification G1U JB6
(56) Documents cited GB 1500695
(58) Field of search G1U
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(54) **Resistance Measuring Circuit**

(57) A resistance measuring circuit comprises a reference resistance 2 and the resistance to be measured 4, connected in series between a constant voltage source V and ground, an integrator being connected as shown in Figure 1 to form a dual range voltmeter. Integration is performed from a threshold level V_T for a fixed time interval T_1, the time T_2 for the integrator to return to the threshold level V_T is then measured. The ratio of the times T_1/T_2 is then proportional to the ratio of the reference and unknown resistances, R_2/R_4.

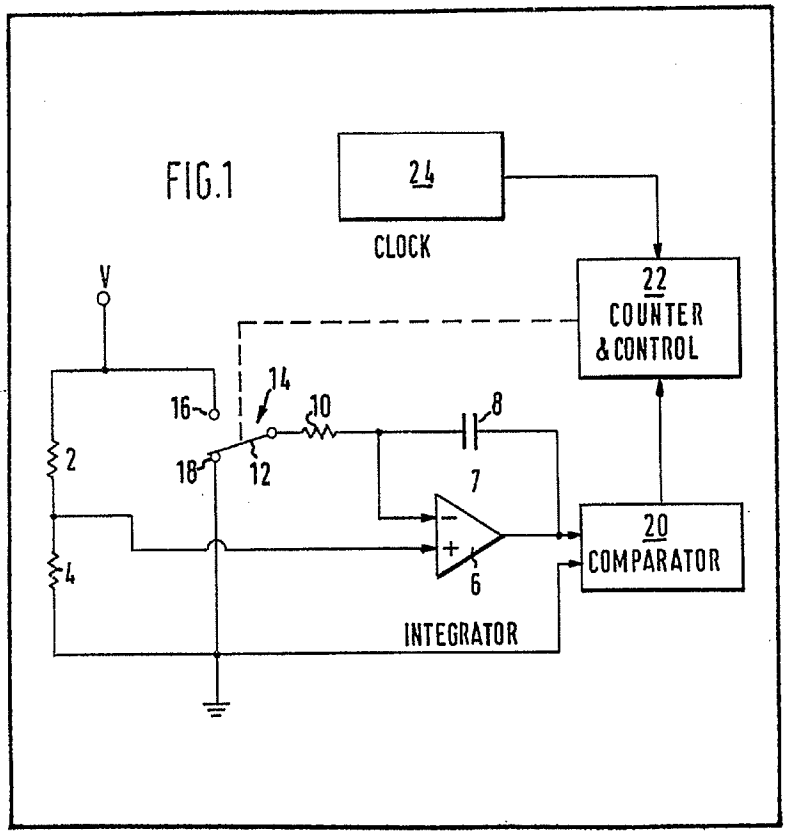

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FIG.1

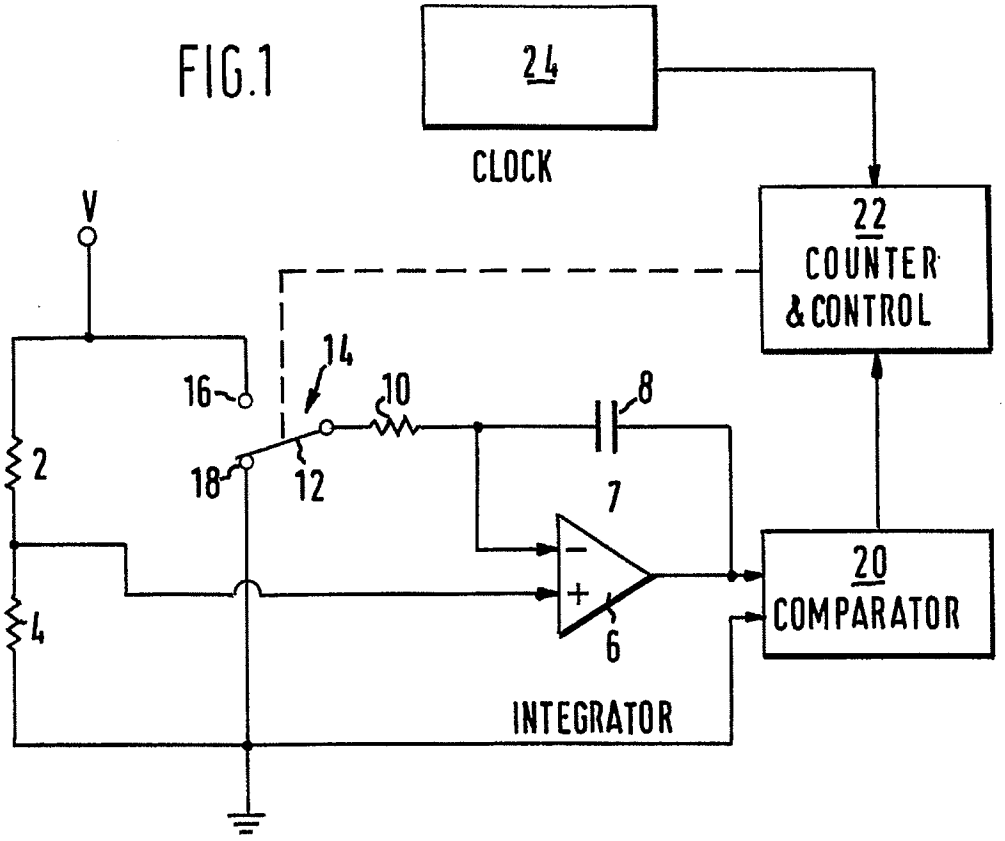
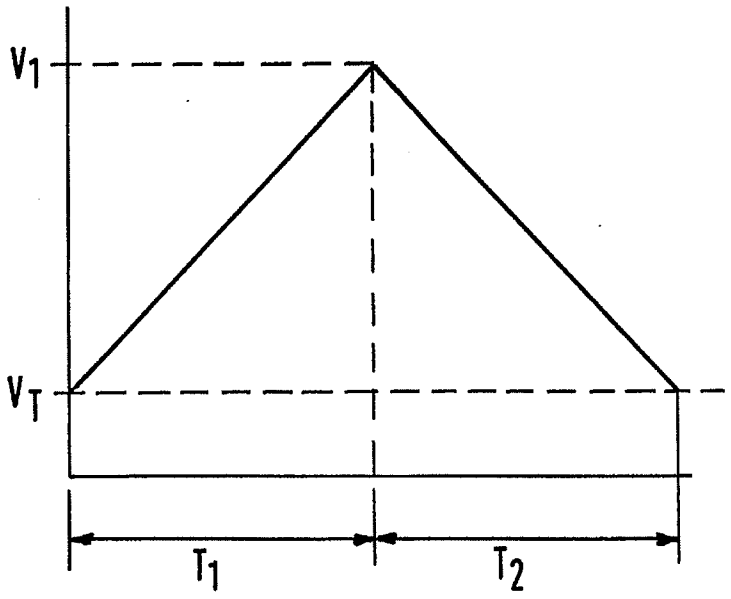

24
CLOCK
22
COUNTER
& CONTROL
V
16
14
10
8
2
18
12
7
4
6
20
COMPARATOR
INTEGRATOR

FIG.2


V_1
V_T
T_1
T_2

SPECIFICATION

Resistance Measuring Circuit

The present invention is directed to a resistance measuring circuit and more specifically to a circuit that provides a digital representation of the resistance being measured.

According to the invention, there is provided a resistance measuring circuit comprising a reference resistance and a resistance to be measured connected in series between a constant voltage source and a circuit ground, an integrator connected to the junction between the resistances, means for producing a first count during a first fixed time period while allowing the integrator to integrate from a fixed threshold level during the first period, and means for producing a second count during a second time period following the first period and having a duration enabling the integrator to return to the fixed threshold level, the circuit being such that the ratio of the first and second counts is proportional to the ratio of the resistance values of the reference and unknown resistances.

An embodiment of the present invention will now be described by way of example only, with reference to the accompanying drawings in which:—

Figure 1 is a block diagram of an example of a resistance measuring circuit according to the present invention and,

Figure 2 is a waveshape drawing of the operation of the integrator used in the circuit shown in Figure 1.

Referring to Figure 1, the resistance measuring circuit includes a known reference resistor 2 and an unknown resistor 4 to be measured connected in series between a supply voltage V and the common or ground connection for the supply voltage V. The resistors 2 and 4, are connected with one end of the reference resistor 2 connected to the supply voltage V and one end of the unknown resistor 4 connected to the common or ground connection. The other ends of the resistors 2, 4 are connected together, and the connection between the series resistors 2 and 4 is connected to the non-inverting input of an operational amplifier 6 arranged in an integrator citcuit 7. The output of the amplifier 6, i.e. the output of the integrator 7, is connected to the inverting input of the amplifier 6 through a feedback capacitor 8. The inverting input of the amplifier 6 is also connected through an input resistor 10 to the movable switch arm 12 of a single pole, double throw switch 14. One switch contact 16 of the switch 14 is connected to the supply voltage V while the other switch contact 18 is connected to the common or ground connection.

The output of the amplifier 6 is also connected to a first input of a signal comparator 20 which is arranged to compare the output of the integrator 7 with the threshold signal applied to a second input of the comparator 20 from the common or ground connection. The output of the comparator 20 is connected to a control input of a counter and control circuit 22. A clock signal generator, or oscillator, 24 is arranged to supply clock signals to the counter and control circuit 22 to be counted by a counter therein. The counter and control circuit 22 is used to control the movement of the switch arm 12 of the switch 14 for example by a relay, to produce a switching of the inverting input of the amplifier 6 between two input signal levels, i.e. the supply voltage ground connection and supply voltage V for a first and second time interval, respectively. Specifically, the first time interval during which the inverting input of the amplifier 6 is connected to the supply voltage ground by the switch 14 is a fixed first time period T_1 as determined by a count of the counter in the counter and the control circuit 22 to a predetermined count. During this first time period, the output of the integrator 7 ramps or increases to a voltage V_1. Upon the attainment of this fixed count, the counter is reset and the switch 14 is actuated by the output signal from the counter and control circuit 22 to switch the switch arm 12 to the switch contact 16. This position of the switch arm 12 is effective to apply the power supply level V to the inverting input of the amplifier 6. The switch arm 12 is retained in contact with the switch contact 16 until the output of the integrator 7 has returned to the common or ground signal level as determined by the comparator 20 during a second time interval T_2. The counter counts clock signals during the second time period, and the second time period count is retained for use as hereinafter discussed.

The operation of the integrator 7 is illustrated in the waveshape diagram shown in Figure 2. Analyzing the operation of the integrator 7, the initial operation during the first fixed time interval T_1 involves the output of the integrator amplifier 6 ramping to a voltage V_1 defined by:

$$V_1 = V_T + \frac{1}{RC} \cdot \int_0^{T_1} \frac{R_x}{R_x + R_{Ref}} \cdot V \, dt$$

which is equal to:

$$V_1 = V_T + \frac{V}{RC} \cdot \frac{R_x}{R_x + R_{Ref}} \cdot T_1$$

where:

T_1 is the fixed time interval switching of switch 14.

R is the input resistor 10.

V_T is the comparator threshold level.

R_x is the unknown resistor R4.

R_{Ref} is the reference resistor R2.

C is the feedback capacitor 8.

The integrator inverting input is then switched to the voltage level of the supply voltage V. The time T_2 required to ramp the output of the amplifier 6 back to the comparator threshold level which is the common or ground level is determined by the equation:

$$V_T = V_1 - \frac{1}{RC} \cdot \int_{T_1}^{T_1+T_2} \frac{R_{Ref}}{R_x+R_{Ref}} \cdot V \cdot dt$$

which is equal to

$$V_T = V_1 - \frac{V}{RC} \cdot \frac{R_{Ref}}{R_x+R_{Ref}} \cdot T_2$$

Solving the above equations for

$$\frac{T_2}{T_1} = \frac{R_x}{R_{Ref}}$$

This relationship is independent of the supply voltage V, the resistor 10, the capacitor 8 and the threshold voltage of the comparator and depends only on the ratio of the unknown resistor 4 to the reference resistor 2. The reference resistor 2 is very stable fixed resistor to assure the accuracy of the measurement of the unknown resistor. The ratio of the time intervals,

$$\frac{T_2}{T_1}$$

is converted to a digital representation by using the fixed and the final count stored in the counter part of the counter and control circuit 22. This conversion does not require a precise clock frequency from the clock circuit 24 since clock frequency must be stable during the time of integration by the integrator amplifier 6. The actual computation of the value of the unknown resistor 4 can be performed by any suitable means, e.g. a microprocessor, etc., such devices being well-known in the art.

Claims

1. A resistance measuring circuit comprising a reference resistance and a resistance to be measured connected in series between a constant voltage source and a circuit ground, an integrator connected to the junction between the resistances, means for producing a first count during a first fixed time period while allowing the integrator to integrate from a fixed threshold level during the first period, and means for producing a second count during a second time period following the first period and having a duration enabling the integrator to return to the fixed threshold level, the circuit being such that the ratio of the first and second counts is proportional to the ratio of the resistance values of the reference and unknown resistances.

2. The resistance measuring circuit of Claim 1, wherein the integrator includes an operational amplifier; and including a switch for selectively connecting the other input of the amplifier either to said voltage source or said circuit ground; a comparator for comparing the output of the amplifier with a circuit ground level signal; a clock signal generator; and counter and control means for counting the clock signals during said first period while energising the switch to connect the other amplifier input to circuit ground and for energising the switch to connect the other amplifier input to the voltage source during the second period.

3. The resistance measuring circuit of Claim 2, wherein the switch includes a relay controlled by said counter and control means.

4. A resistance measuring circuit substantially as herein described with reference to, and as illustrated in, the accompanying drawings.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1981. Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.